

ASSP

Single Chip 8-Bit A/D and 9-Bit D/A Converter

MB40168/MB40178

DESCRIPTION

The Fujitsu MB40168 and MB40178 are high speed, low power single chip A/D and D/A converters designed for video processing applications. The A/D converter has a resolution of 8 bits while the D/A converter has 9-bit resolution. They are fabricated in Fujitsu's advanced bipolar technology, and housed in a 48-pin plastic shrink DIP or 44-pin plastic QFP package.

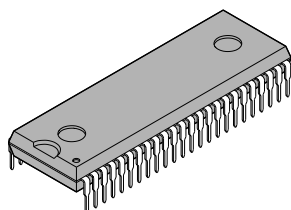
FEATURES

- Resolution A/D: 8 bits
 D/A: 9 bits
- Conversion Rate A/D: Max. 20 MSPS
 D/A: Max. 40 MSPS
- Linearity Error A/D: Max. + 0.3%
 D/A: Max. + 0.2%
- On-chip reference voltage generator (resistor divided method) and clamp circuit
- Analog Input Voltage 3 to 5 V without clamp circuit
 0 to 3 V in 1.95 V_{P-P} clamp circuit
- Analog Output Voltage 3 to 5 V

(Continued)

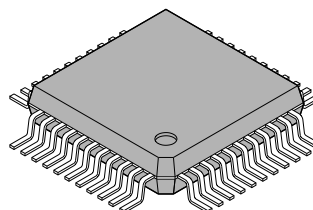
PACKAGES

48 pin, Plastic SH-DIP



(DIP-48P-M01)

44 pin, Plastic QFP



(FPT-44P-M11)

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

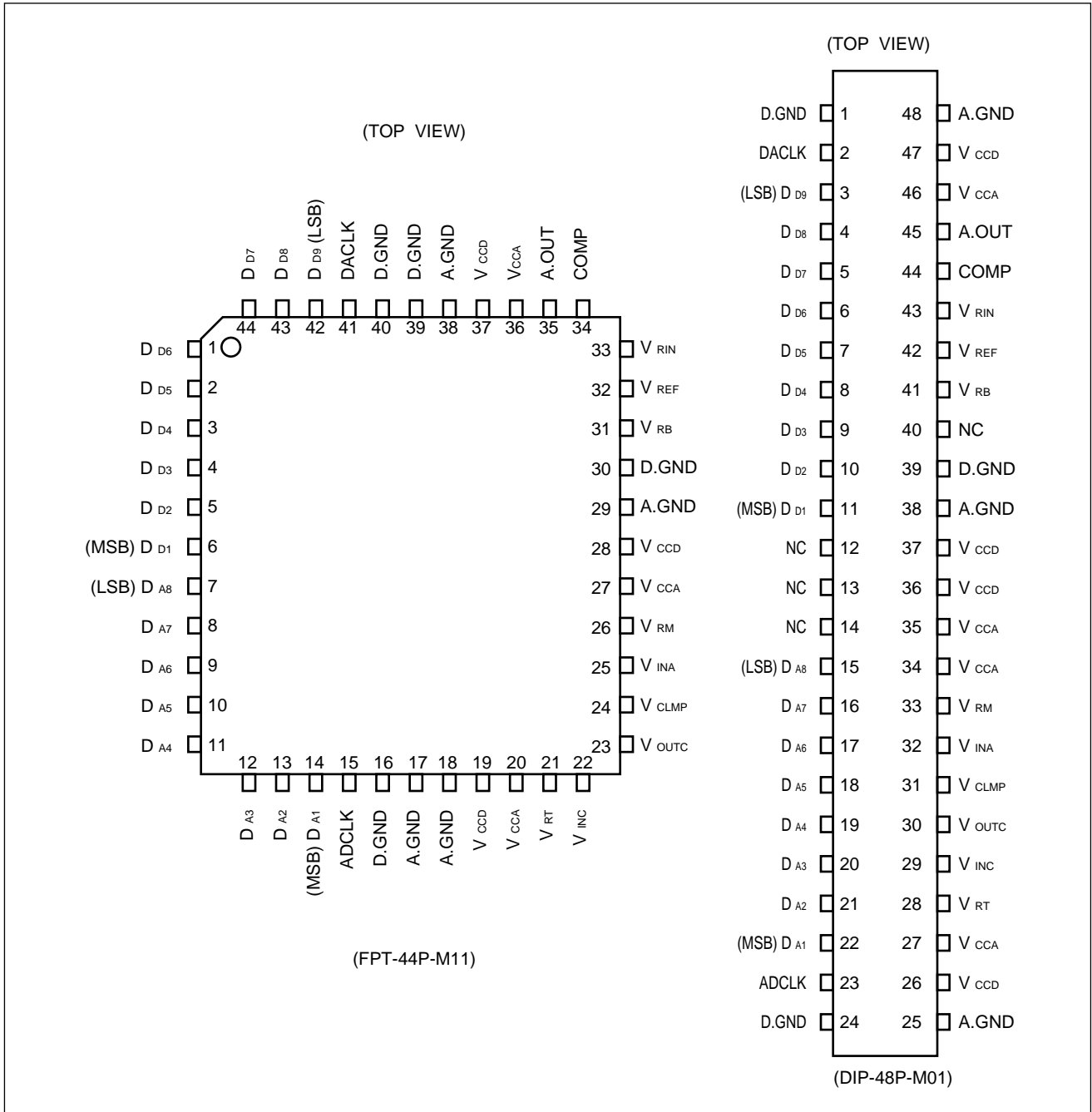
MB40168/MB40178

(Continued)

- Digital Input/Output Interface
 - Power Supply Voltage
 - Power Dissipation
 - Package Options
- TTL Levels
 + 5.0 V single power supply
 Typ. 350 mW
 48-pin Plastic Shrink DIP/
 44-pin Plastic QFP Package

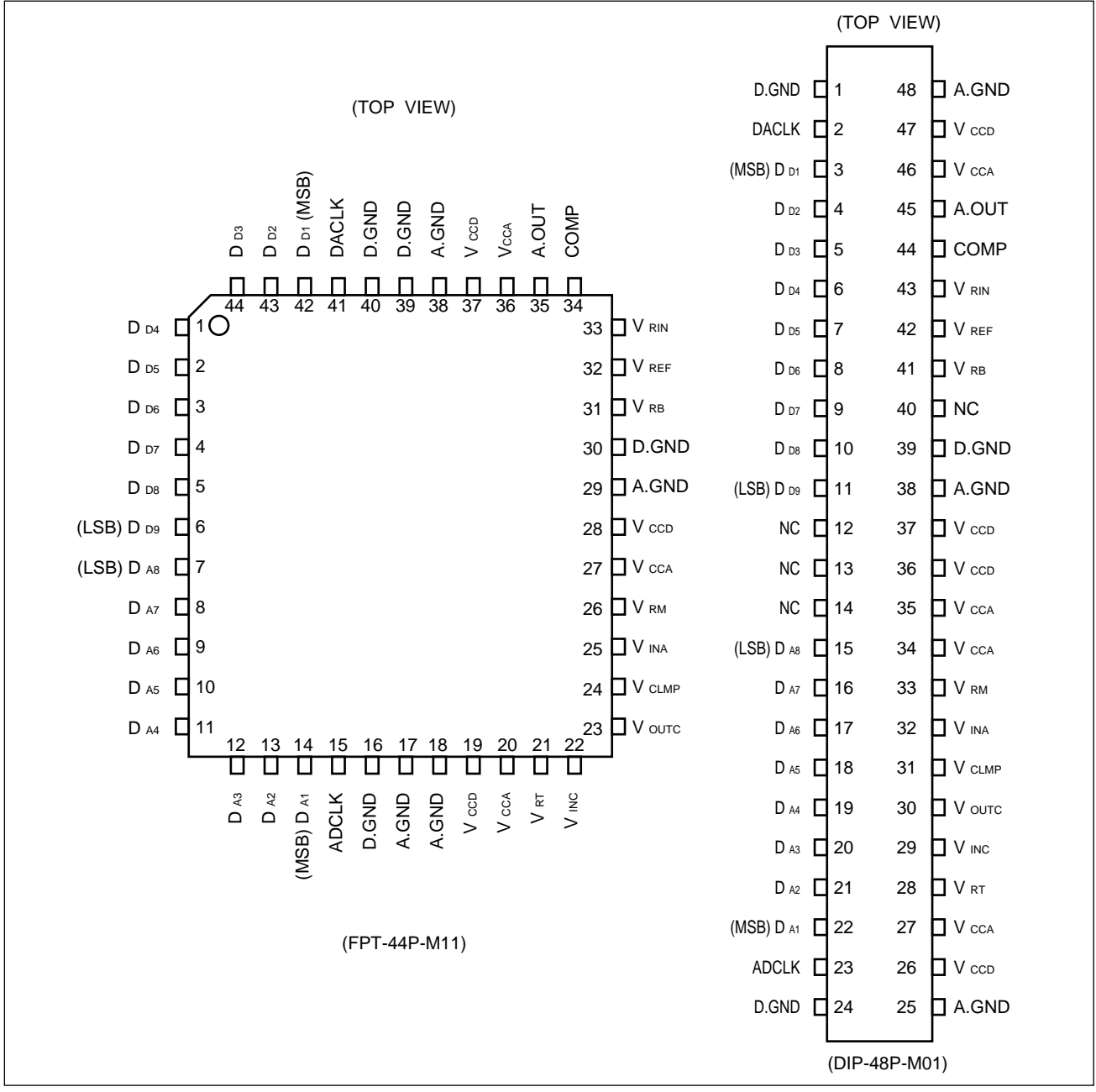
■ PIN ASSIGNMENTS

- MB40168



MB40168/MB40178

• MB40178



MB40168/MB40178

■ PIN DESCRIPTION

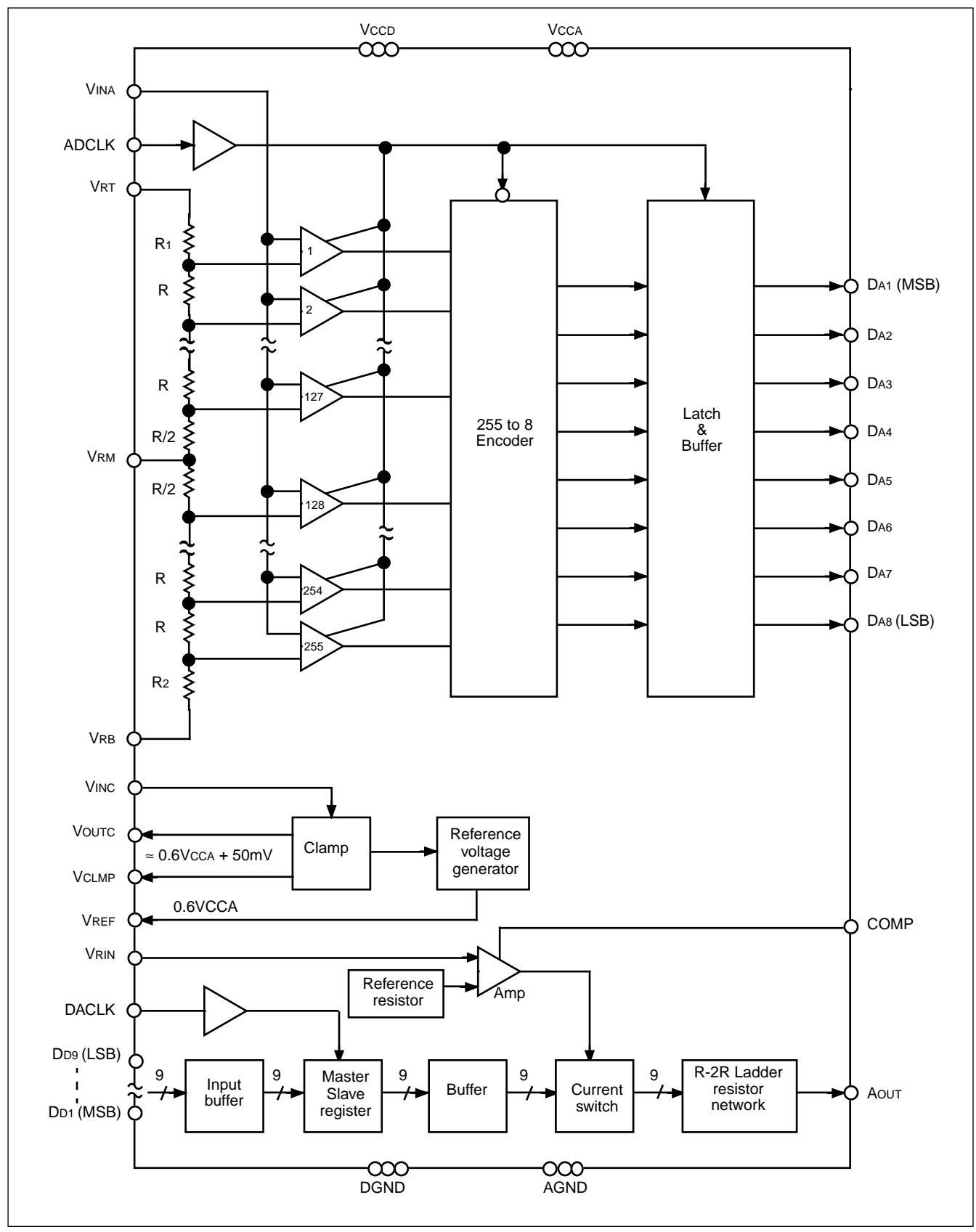
Symbol	Pin No.		I/O	Name & Function
	QFP-44	SH-DIP-48		
VCCD	19, 28, 37	26, 36, 37, 47	—	Digital Power Supply pins (+ 5 V).
VCCA	20, 27, 36	27, 34, 35, 46	—	Analog Power Supply pins (+ 5 V).
DGND	16, 30, 39, 40	1, 24, 39	—	Digital Ground (0 V). These pins should be connected to the analog ground on the application system.
AGND	17, 18, 29, 38	25, 38, 48	—	Analog Ground (0 V). These pins should be connected to the analog ground on the application system.
DA8 - DA1	7 - 14	15 - 22	O	ADC Digital Output pins. TTL level.
ADCLK	15	23	I	ADC Clock Input pin. TTL level.
VRT	21	28	I	ADC Reference Voltage Input pin. (5 V Input)
VINC	22	29	I	Sync Tip Clamp Circuit Analog Input pin. (0 - 3 V, 1.95 VP-P). When a clamp circuit is not used, this pin is connected to ground.
VOUTC	23	30	O	Clamp Circuit Analog Output pin. It is used by adding a capacitor (1 μ F or more) between VCLMP and VOVTC pins. When a clamp circuit is not used, this pin is left open.
VCLMP	24	31	O	Clamp Voltage Output pin (3.05V Output). When a clamp circuit is not used, this pin is left open.
VINA	25	32	I	ADC Analog Signal Input pin. (3 - 5 V)
VRM	26	33	—	ADC Middle Reference Voltage Monitor pin. (Mid of VRT - VRB is set to this pin). Normally this pin is left open.
VRB	31	41	I	ADC Reference Voltage Input pin. (3 V)
VREF	32	42	O	Reference Voltage Output pin. (Resistor Divider, 3 V) By connecting this pin to VRB pin, 3V Voltages are generated. When a reference voltage is not used, this pin is left open.
VRIN	33	43	I	DAC Reference Voltage Input pin (3 V)
COMP	34	44	—	Phase Compensation Capacitor pin. (Capacitor greater than 0.1 μ F should be connected between this pin and Analog Ground.)
AOUT	35	45	O	Analog Signal Output pin
DACLK	41	2	I	DAC Clock Input pin. TTL level.
DD9 - DD1	1 - 6 *1 42 - 44	3 - 11*2	I	DAC Digital Data Input pins. TTL level.

*1: MB40168 (MSB: 6 pin, LSB: 42 pin), MB40178 (MSB: 42 pin, LSB: 6 pin)

*2: MB40168 (MSB: 11 pin, LSB: 3 pin), MB40178 (MSB: 3 pin, LSB: 11 pin)

MB40168/MB40178

■ BLOCKDIAGRAM



MB40168/MB40178

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V _{CCA} , V _{CCD}	-0.5 to 7.0	V
Analog input voltage	V _{INA}	-0.5 to V _{CC} + 0.5	V
Reference voltage	V _{RT} , V _{RB} , V _{RIN}	-0.5 to V _{CC} + 0.5	V
Clamp circuit input voltage	V _{INC}	-0.5 to V _{CC} + 0.5	V
Digital input voltage	V _{IND}	-0.5 to 7.0	V
Storage temperature	T _{STG}	-55 to +125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MB40168/MB40178

■ RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Value			Unit
			Min.	Typ.	Max.	
Power supply voltage *1		VCCA, VCCD	4.75	5.00	5.25	V
Clamp circuit input voltage *2		VINC	0	—	3	V
Analog input voltage		VINA	VRB	—	VRT	V
ADC reference voltage *3	Top	VRT	VCCA - 0.1	VCCA	VCCA + 0.1	V
	Bottom	VRB	2.75	3.0	3.25	V
DAC reference voltage		VCCA - VRIN	0.7	2.0	2.2	V
		VRIN	2.65	3.0	4.3	V
Digital input high voltage		VIHD	2.0	—	—	V
Digital input low voltage		VILD	—	—	0.8	V
Digital output high current		IOH	-400	—	—	μA
Digital output low current		IOL	—	—	1.6	mA
Clock frequency	A/D	fCLKAD	—	—	20	MHz
	D/A	fCLKDA	—	—	40	MHz
Minimum high clock pulse width	A/D	tWHAD	22.5	—	—	ns
	D/A	tWHDA	10.5	—	—	ns
Minimum Low clock pulse width	A/D	tWLAD	22.5	—	—	ns
	D/A	tWLAD	10.5	—	—	ns
Set up time		tsu	10	—	—	ns
Hold time		tH	4	—	—	ns
Clamp capacitance		CCLMP	1	—	—	μF
Phase compensation capacitance		CCOMP	0.1	—	—	μF
Ambient operating temperature		Ta	-20	—	+70	°C

*1: VCCA and VCCD must be used in the same voltage level.

*2: VINC must have an amplitude of VRT - VCLMP.

*3: VRT - VRB must have 2.0V±0.1V.

MB40168/MB40178

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

- Analog Block

($V_{CCA} = V_{CCD} = 4.75\text{ V to }5.25\text{ V}$, $T_a = -20\text{ °C to }+70\text{ °C}$)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
ADC resolution	—	—	—	8	—	bits
DAC resolution	—	—	—	9	—	bits
ADC linearity error	LEAD	DC accuracy $V_{CCA} = V_{CCD} = 5.0\text{ V}$	—	± 0.15	± 0.3	%
DAC linearity error	LEDA		—	± 0.1	± 0.2	%
Analog input equivalent impedance	R_{INA}	$R_{INA} = \frac{V_{RT} - V_{RB}}{I_{HA} - I_{LA}}$	0.3	1.3	—	$M\Omega$
Analog input capacitance	C_{INA}	$f_{INA} = 1\text{ MHz}$	—	40	—	pF
Analog input high current	I_{HA}	$V_{INA} = V_{RT}$	—	—	45	μA
Analog input low current	I_{LA}	$V_{INA} = V_{RB}$	—	—	40	μA
Reference output voltage	V_{REF}	V_{REF}, V_{RB}, V_{RIN} shorted together	$0.6V_{CCA} - 0.1$	$0.6V_{CCA}$	$0.6V_{CCA} + 0.1$	V
Clamp voltage	V_{CLMP}	—	—	$V_{REF} + 50\text{ mV}$	—	V
ADC reference current	I_{RB}	—	-8.5	-5.5	-3.0	mA
DAC reference current	I_{RIN}	$V_{RIN} = 3.000\text{ V}$	—	—	10	μA
Clamp circuit input current	I_{INC}	$V_{INC} = 0\text{ V}$	-600	-200	—	μA
Full scale output voltage	V_{OFS}	—	$V_{CCA} - 20\text{ mV}$	V_{CCA}	—	V
Zero scale output voltage	V_{OZS}	$V_{CCA} = 5.00\text{ V}$ $V_{CCD} = 5.00\text{ V}$ $V_{RIN} = 3.000\text{ V}$	2.934	3.004	3.072	V
Output impedance	R_o	$T_a = +25\text{ °C}$	192	240	288	Ω
Supply current	I_{CC}	—	—	70	125	mA

MB40168/MB40178

- Digital Block

(V_{CCA} = V_{CCD} = 4.75 V to 5.25 V, T_a = -20 °C to +70 °C)

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Digital output high voltage	V _{OHD}	I _{OH} = -400 μA	2.7	—	—	V
Digital output low voltage	V _{OLD}	I _{OL} = 1.6 mA	—	—	0.4	V
Digital input high voltage	V _{IHD}	—	2.0	—	—	V
Digital input low voltage	V _{ILD}	—	—	—	0.8	V
Digital input high current	I _{IHD}	V _{IHD} = 2.7 V	—	—	20	μA
Digital input low current	I _{ILD}	V _{ILD} = 0.4 V	-100	—	—	μA

2. AC CHARACTERISTICS

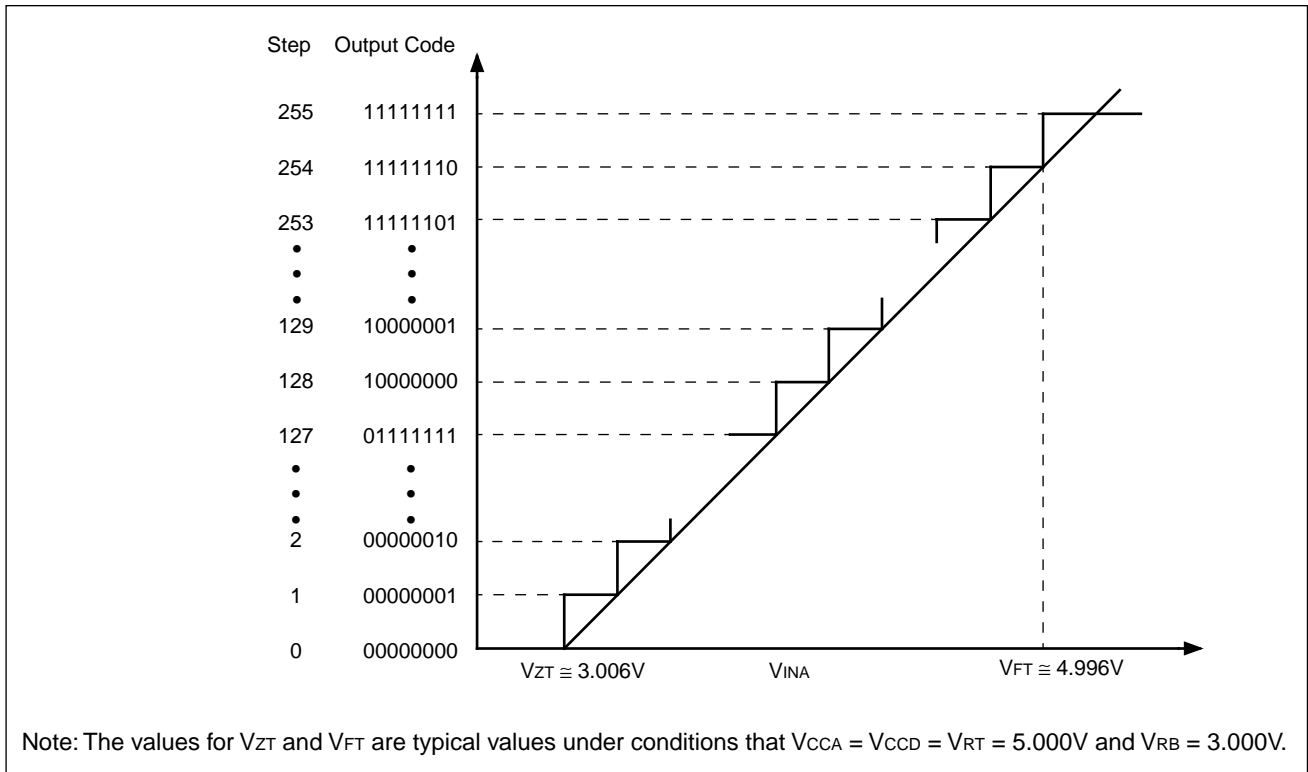
(V_{CCA} = V_{CCD} = 4.75 V to 5.25 V, T_a = -20 °C to +70 °C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Maximum conversion rate	A/D	f _{SAD}	—	20	—	—	MSPS
	D/A	f _{SDA}	—	40	—	—	MSPS
Digital output delay time		t _{pd AD}	—	8	15	30	ns
Analog output delay time		t _{pd DA}	C _L = 15 pF	—	10	—	ns
Analog output rise time		t _r		—	5	—	ns
Analog output fall time		t _f	Terminating resistor	—	5	—	ns
Settling time		t _{set LH} , t _{set HL}	A _{OUT} = 240 Ω	—	16	—	ns

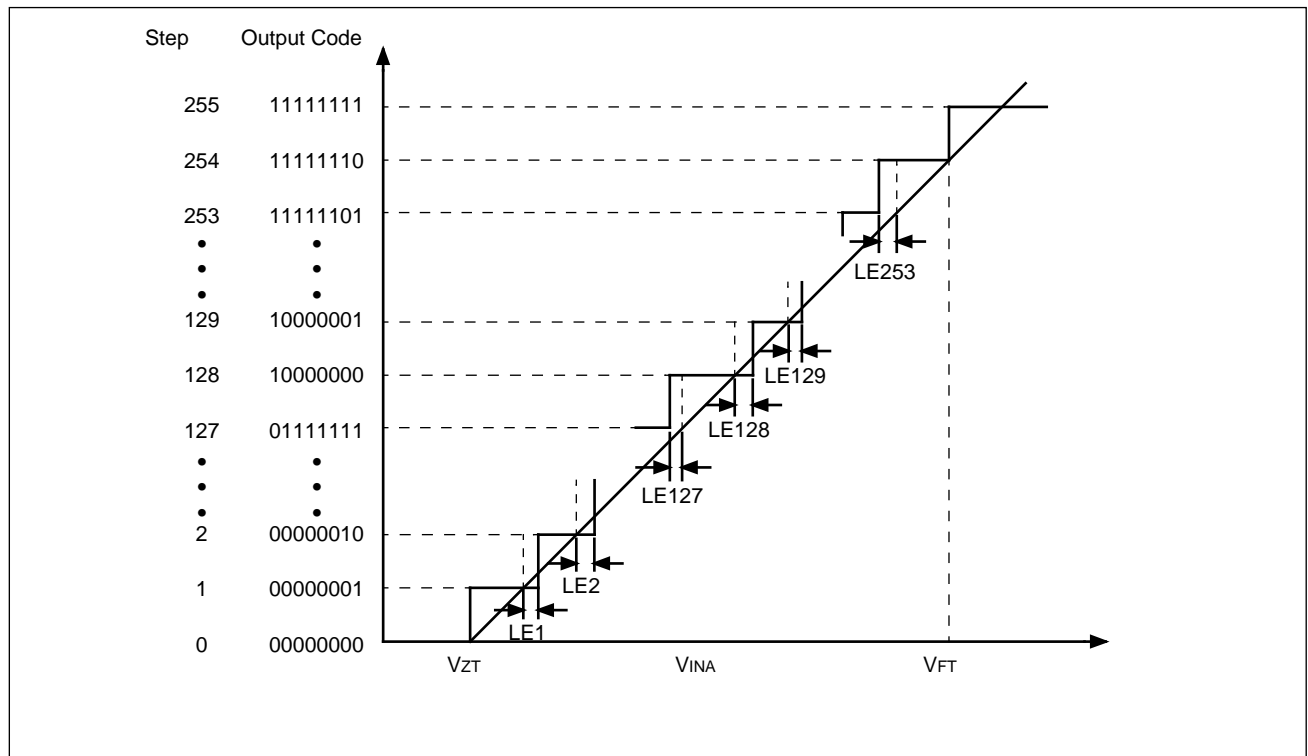
MB40168/MB40178

LINEARITY ERROR OF A/D CONVERSION

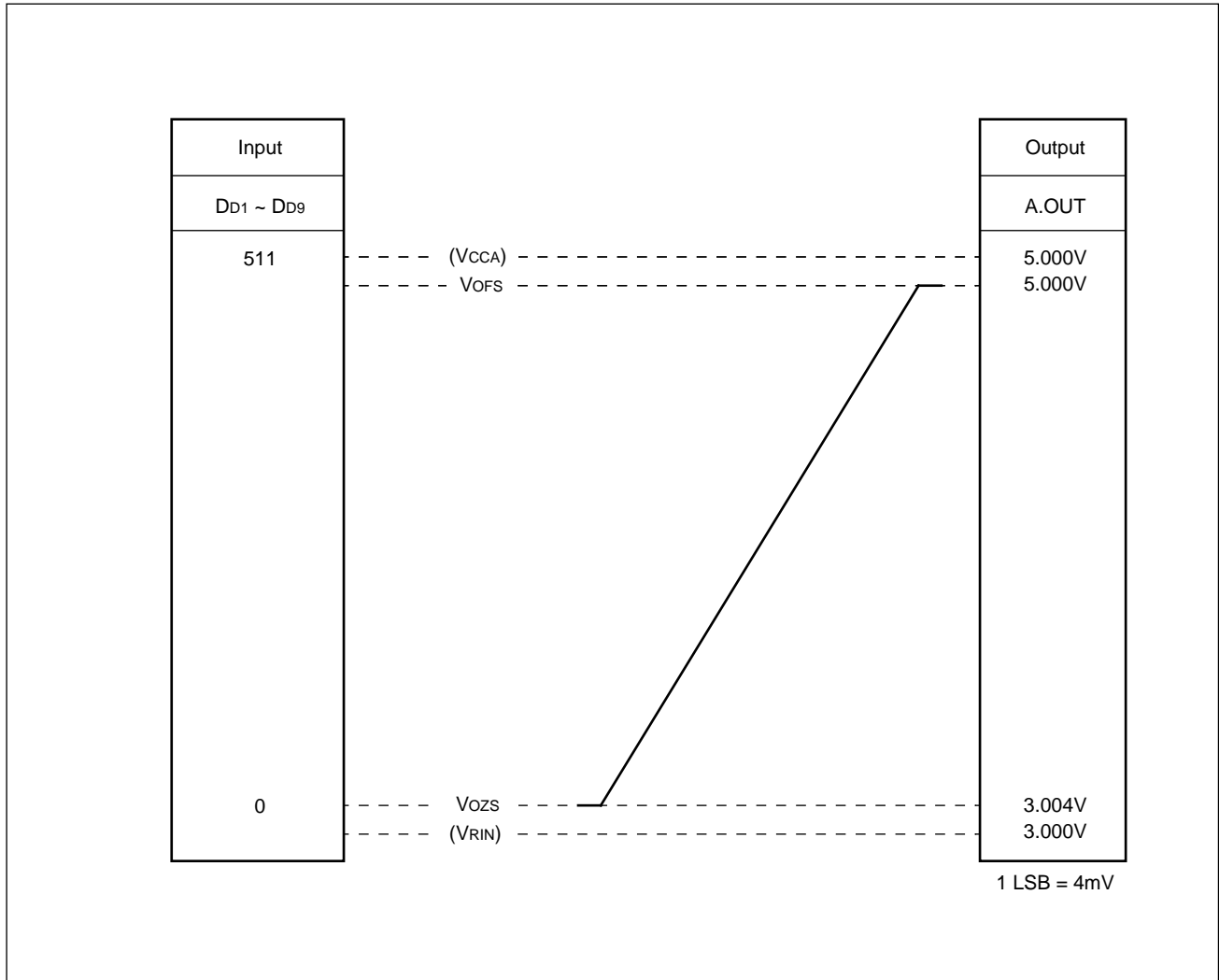
• Ideal Characteristic



• Actual Characteristic



■ OUTPUT VOLTAGE CHARACTERISTIC OF D/A CONVERTER BLOCK



■ CALCULATION OF DAC OUTPUT VOLTAGE WHEN THE IDEAL CONVERSION IS PERFORMED

$$AOUT_N = V_{CCA} - \frac{511-N}{512} \times (V_{CCA} - V_{RIN})$$

(N: Digital code (0 ~ 511))

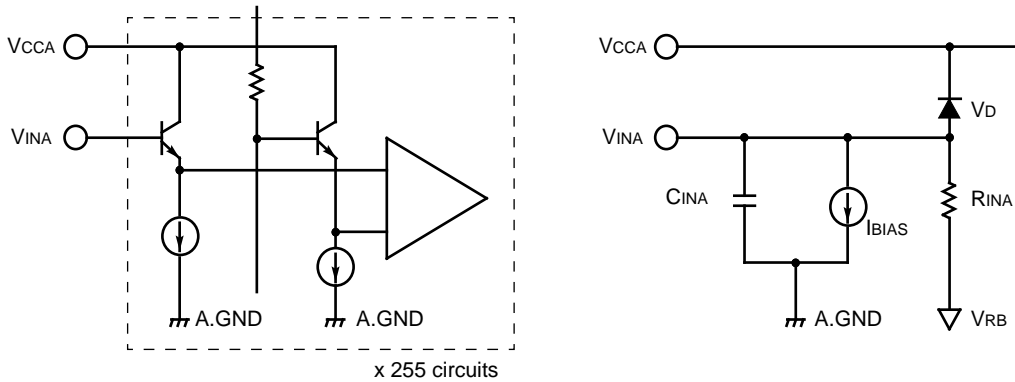
$$V_{OFS} = V_{CCA}$$

$$V_{OZS} = V_{CCA} - \frac{511}{512} \times (V_{CCA} - V_{RIN})$$

MB40168/MB40178

■ EQUIVALENT CIRCUITS OF ADC BLOCK

• Analog Input Equivalent Circuit



CINA: Junction Capacitance of non-linear emitter follower

RINA: Linear resistance model of input current by the comparator switching

VINA < VRB: ∞

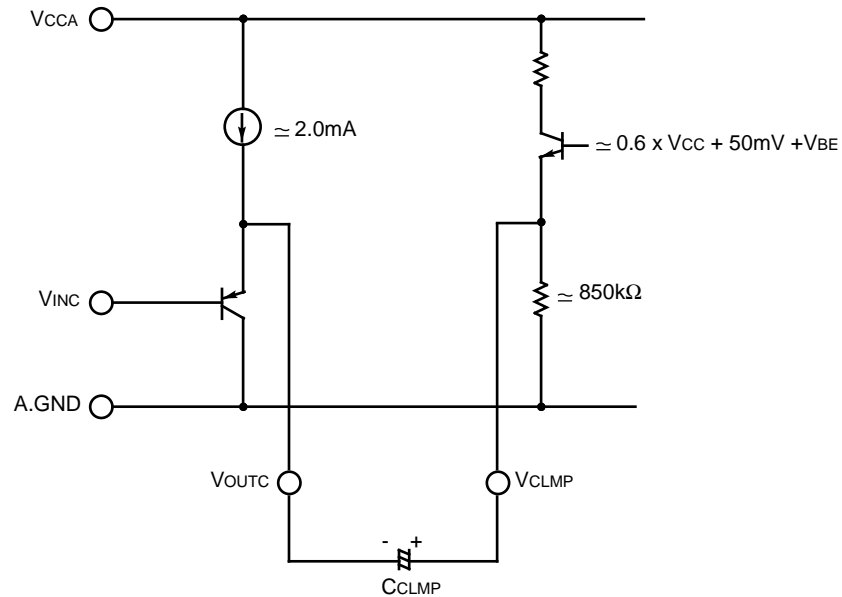
CLK = "H": ∞

VRB: This is the voltage on VRB Pin, not VRB Pin itself.

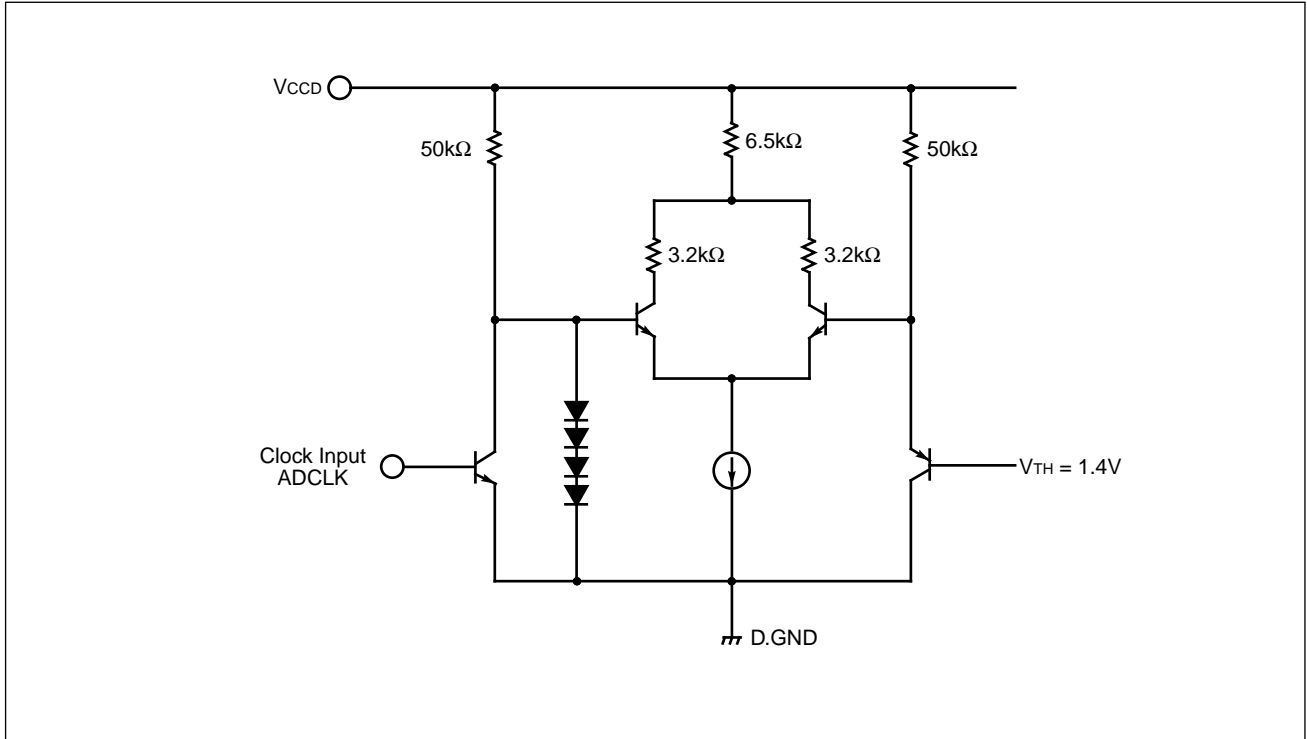
IBIAS: Constant input bias current

Vd: Base-Collector junction diode of emitter follower transistor

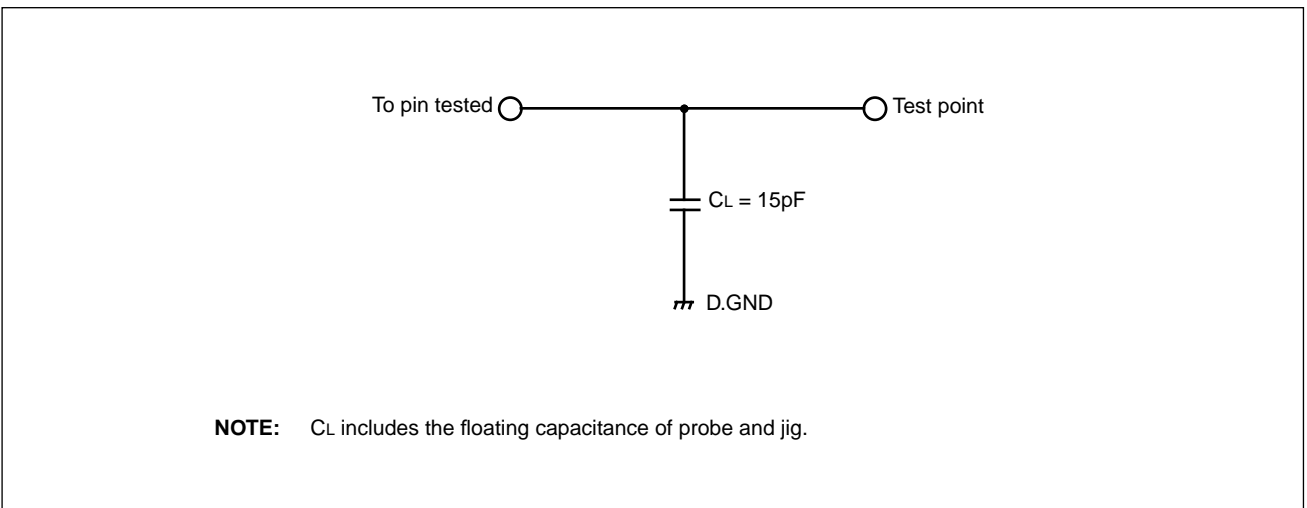
• Clamp Input Equivalent Circuit



- Digital Input Equivalent Circuit



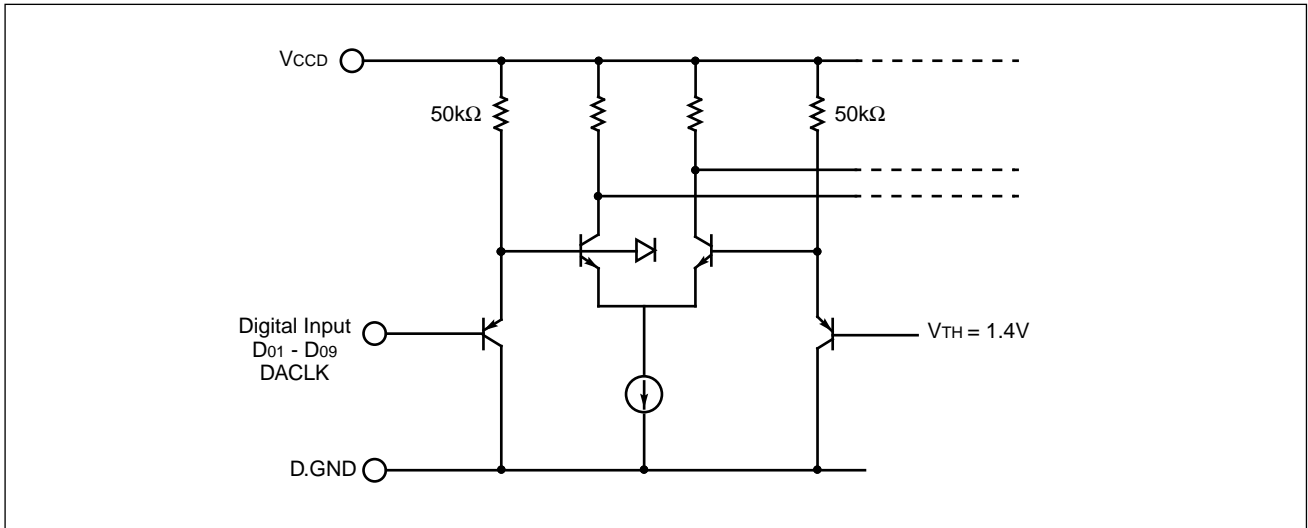
- Digital Output Load Circuit



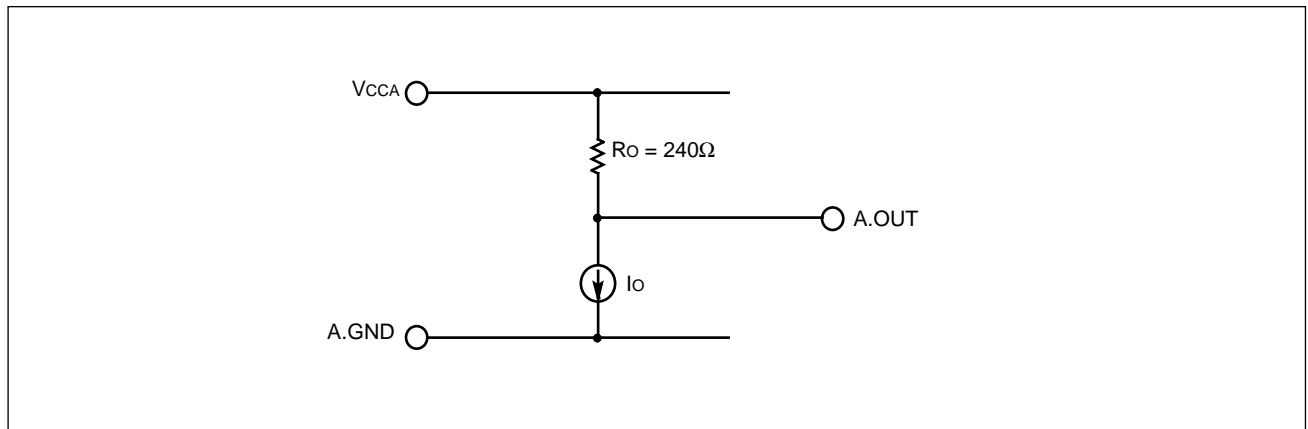
MB40168/MB40178

■ EQUIVALENT CIRCUITS OF DAC BLOCK

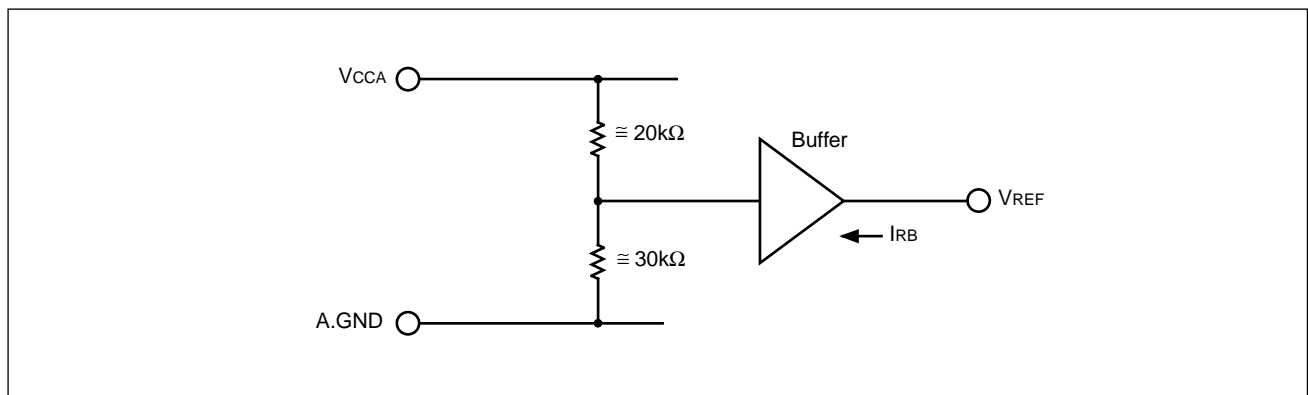
• Digital Input Equivalent Circuit



• Analog Output Equivalent Circuit



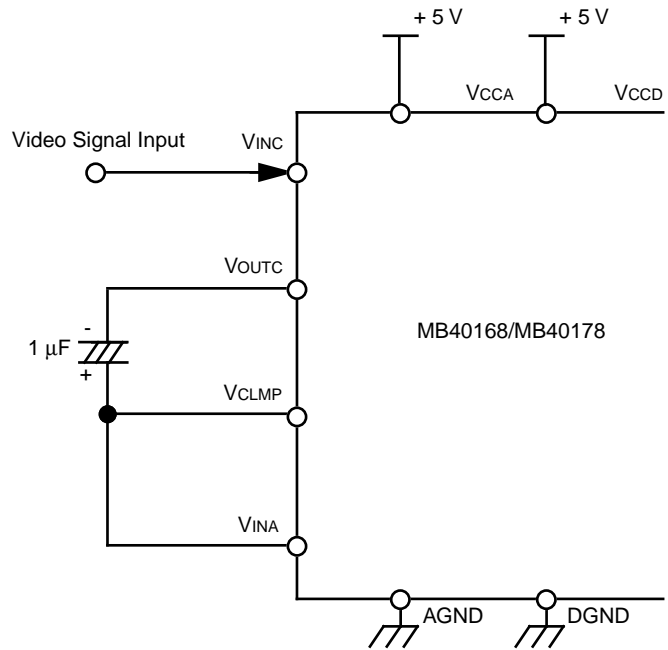
• Reference Voltage Generator Equivalent Circuit



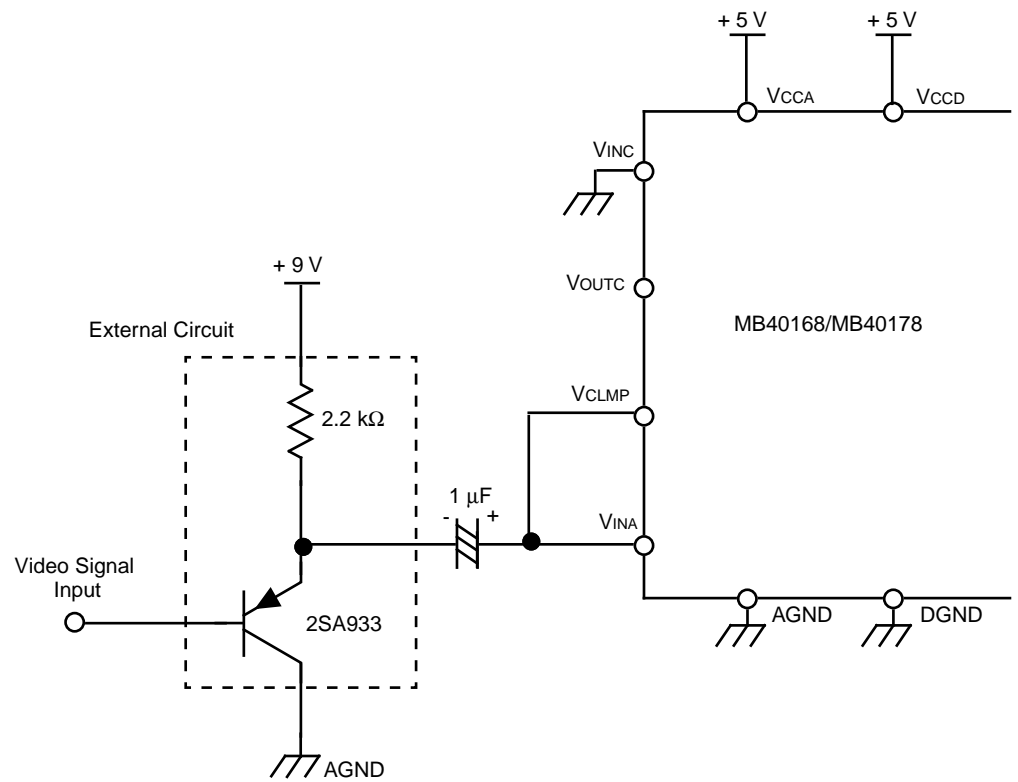
MB40168/MB40178

■ TYPICAL CONNECTION CIRCUITS

Example 1: Video Signal Input to VINC Pin

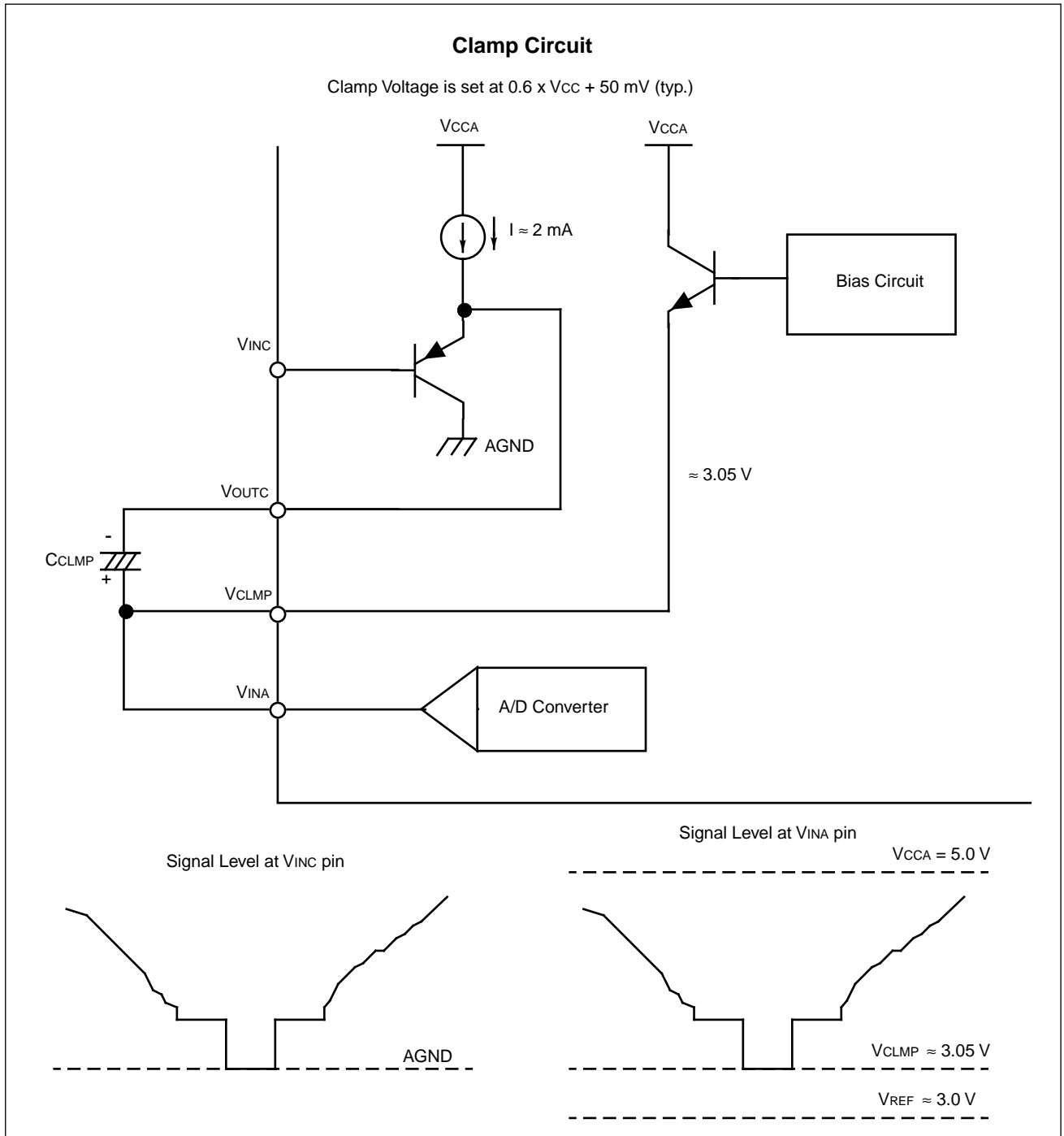


Example 2: Video Signal Input to VCLMP and VINA Pins



MB40168/MB40178

■ CLAMP CIRCUIT OPERATION

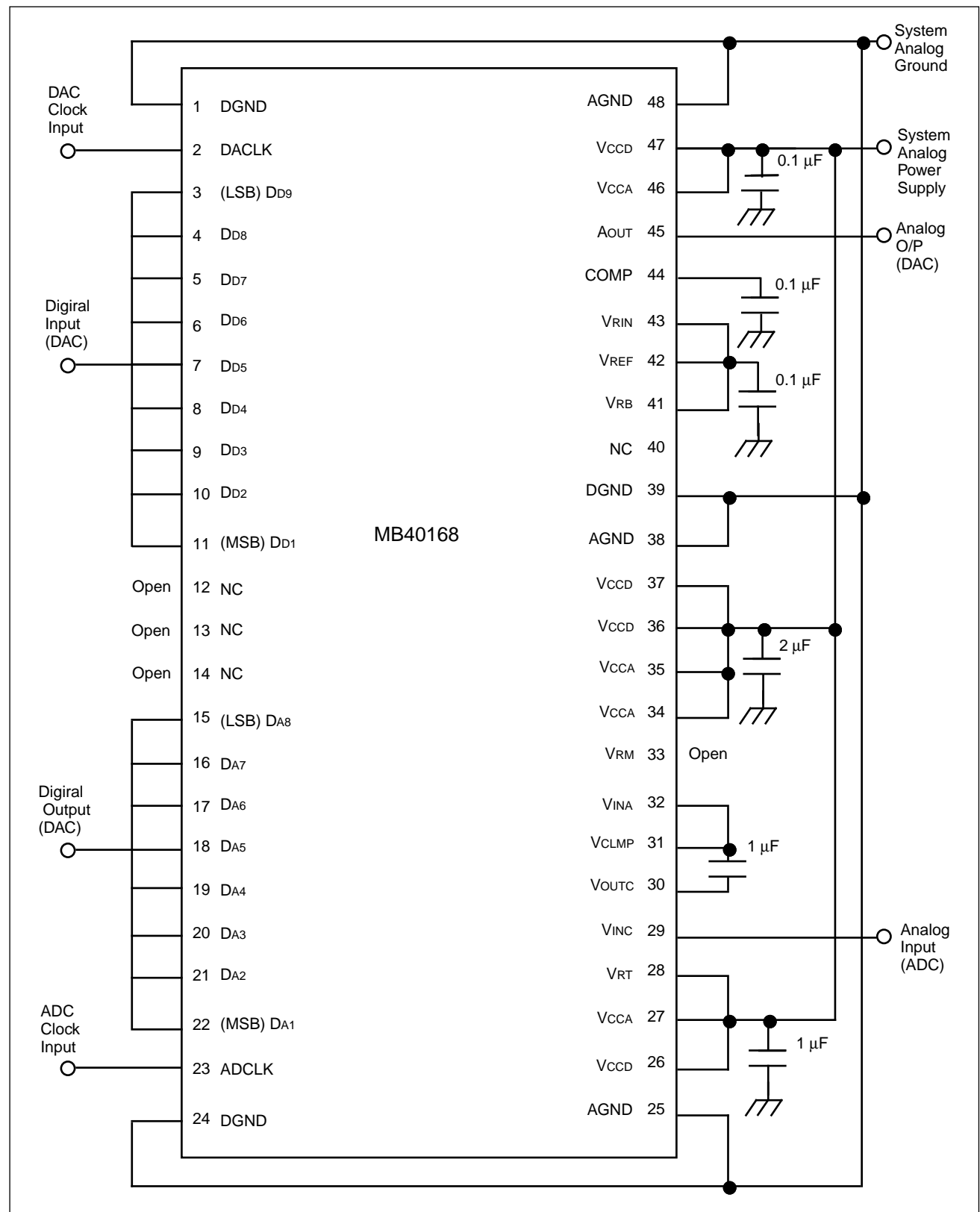


Note: When Clamp Circuit is not applied the signals should be connected as follows:

VINC: Connect to GND.
 VOUTC: Leave open.
 VCLMP: Leave open.

MB40168/MB40178

■ TYPICAL CONNECTION CIRCUIT(Example)



MB40168/MB40178

■ NOTES ON PCB LAYOUT

Power Supply Lines

The device's power supply lines (V_{CCA} , V_{CCD} , AGND and DGND) should be laid out as analog lines and should be separated in so far as possible from other digital lines in order to reduce noise. Also the track widths of these lines should be as wide as possible to reduce parasitic impedance.

Coupling Capacitors

The device's power supply lines V_{CCA} and V_{CCD} and the reference voltage pins V_{RIN} , V_{REF} , V_{RB} , and V_{RT} should be decoupled to analog ground by means of approx. 1 μ F capacitors which should be placed as close as possible to these pins.

Digital Output Load

The load at the digital outputs should be kept as low as possible to prevent noise in the power supply lines caused by digital output switching. If, due to long wiring, the load becomes large then a buffer with small input capacitance should be inserted to reduce load capacitance.

■ OTHER NOTES ON OPERATION

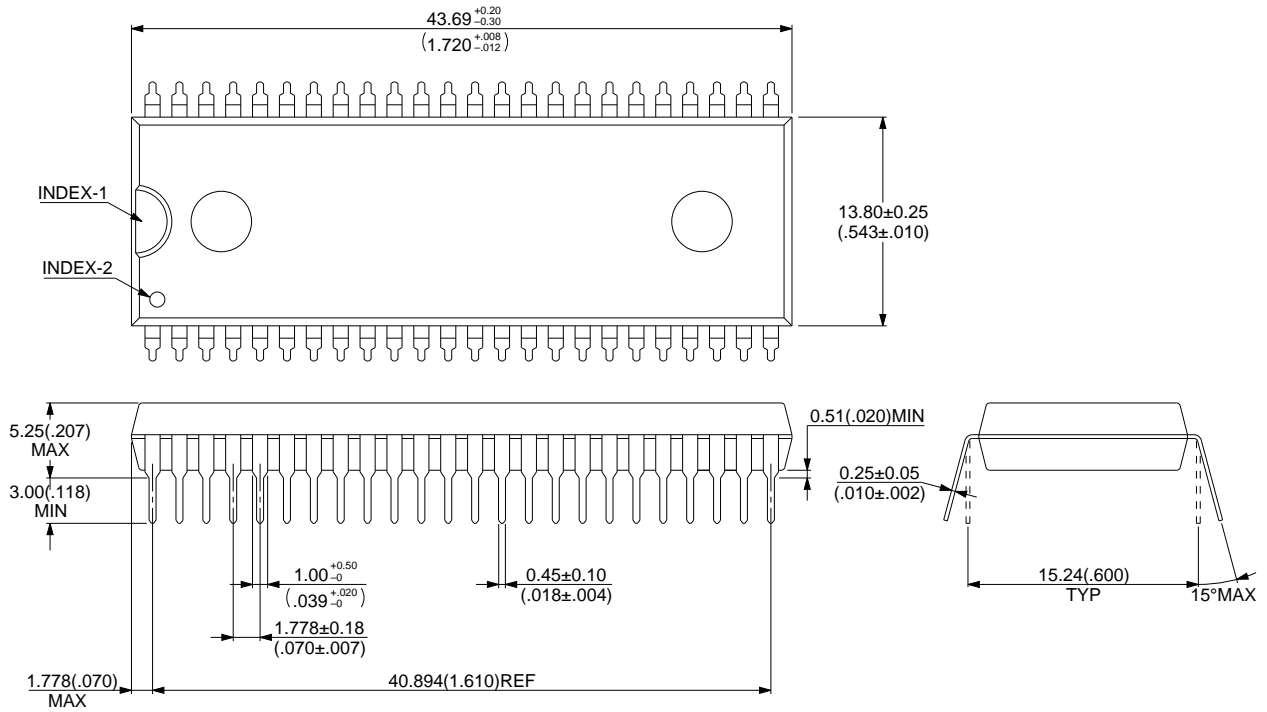
When using the D/A converter with its V_{RIN} pin connected to the V_{REF} pin, the A/D converter's V_{RB} pin must also be connected to the V_{REF} because otherwise the internal reference voltage generation circuitry cannot output 3 V.

When using the D/A converter with 8 bit resolution the DD9 (LSB) pin should be grounded.

MB40168/MB40178

■ PACKAGE DIMENSIONS

48 pin, Plastic SH-DIP
(DIP-48P-M01)



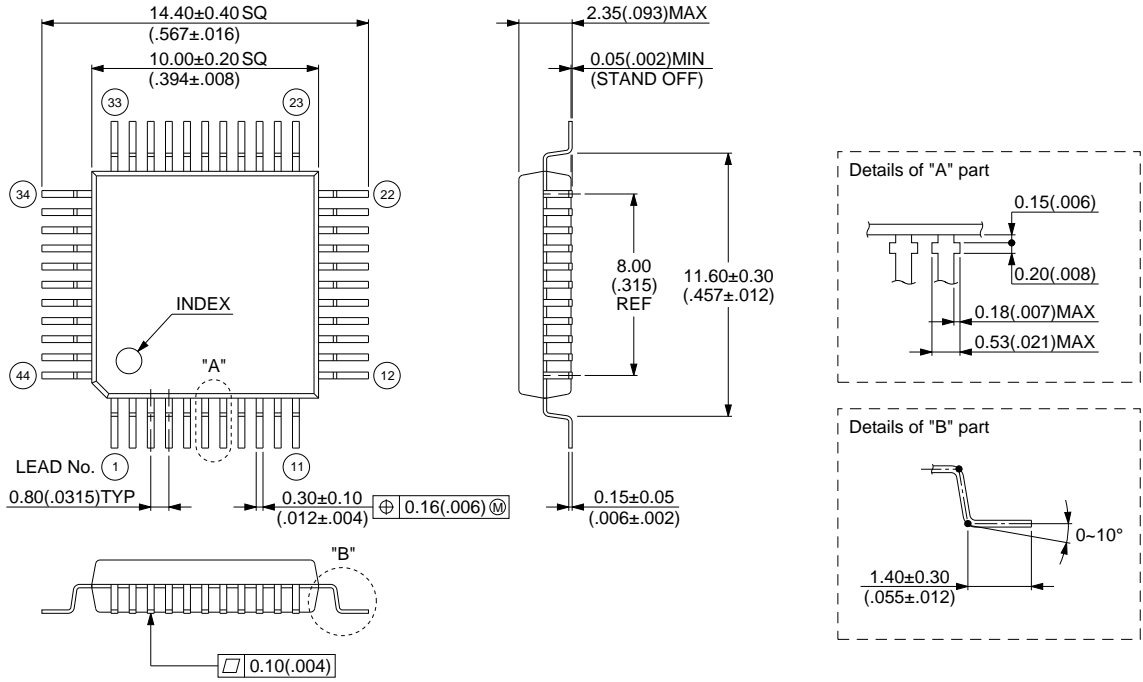
© 1994 FUJITSU LIMITED D48002S-3C-3

Dimensions in mm (inches).

(Continued)

MB40168/MB40178

44 pin, Plastic QFP
(FPT-44P-M11)



MB40168/MB40178

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka
Nakahara-ku, Kawasaki-shi
Kanagawa 211-88, Japan
Tel: (044) 754-3753
Fax: (044) 754-3329

North and South America

FUJITSU MICROELECTRONICS, INC.
Semiconductor Division
3545 North First Street
San Jose, CA 95134-1804, U.S.A.
Tel: (408) 922-9000
Fax: (408) 432-9044/9045

Europe

FUJITSU MIKROELEKTRONIK GmbH
Am Siebenstein 6-10
63303 Dreieich-Buchsschlag
Germany
Tel: (06103) 690-0
Fax: (06103) 690-122

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LIMITED
#05-08, 151 Lorong Chuan
New Tech Park
Singapore 556741
Tel: (65) 281 0770
Fax: (65) 281 0220

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

FUJITSU semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION:

Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.

F9703

© FUJITSU LIMITED Printed in Japan